X-BAND RECEIVER PROTECTOR USING GLASS TECHNOLOGY

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Abstract

This paper describes a receiver protector providing passive limiting and active switching for an X-band phased array radar. The 1650 μm x 4440 μm circuit uses a glass integrated circuit process and discrete PIN diodes to achieve:

Loss: 1.0 dB
VSWR: 1.25:1
Isolation: 40 dB
Power Handling: 10W CW

Introduction

Solid state phased array radar systems are used in many military and commercial applications. Each channel typically contains an LNA to amplify low level incoming signals. This device is sensitive and can be damaged by high power signals.

Since each channel has transmit and receive capability, some of the transmit power will leak into the receive channel. In this case, the receiver protection is accomplished with active switching. If unpredictable high power signals are present, the antenna will transmit a signal into the receiver channel where it can cause damage. Since this may occur when the system is inoperative, this protection must be passive.

This paper describes an integrated circuit that performs this active switching and passive limiting receiver protector function. The integrated circuit medium is M/A-COM's glass process. The process brings silicon vias to the surface of a glass wafer. These highly doped, single crystal silicon structures result in low electrical and thermal resistance paths to ground.

The glass is a low loss dielectric (ε_r = 4.1) that supports thin film batch processing techniques. This processing produces passive circuit structures such as transmission lines, spiral inductors, resistors, airbridges and MIM capacitors. The resulting chip is not truly monolithic because discrete semiconductors must be added. The advantage is that performance can be optimized with the discrete components, while maintaining many of the features of an integrated circuit.

Design

To provide passive and active protection, the receiver protector must function as an SPST switch and a passive limiter. The most critical design requirements are low insertion loss and high (10 W CW) power handling capability. A Schottky coupled limiter approach is the basis for the design. The coupled power forward biases the Schottky, which supplies current to the PIN limiter diodes. The topology for this limiter appears in Figure 1.

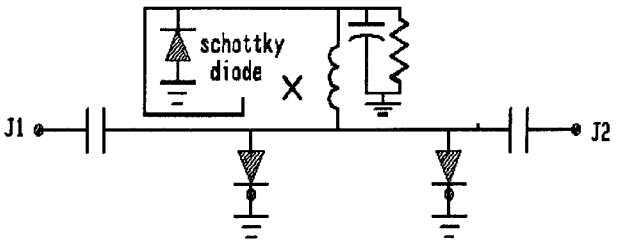

Figure 1: Schottky Coupled Limiter

This particular requirement operates from a single *negative* supply for active switching. To satisfy this,

the PIN diode mounts on a capacitor providing RF ground and DC isolation. The diode bias is supplied at the cathode.

During active operation, the Schottky diode is reverse biased when the receiver protector is in the isolation state. Insertion loss is achieved with a 0 volt bias. In the case of passive limiting, the incident power forward biases the Schottky diode, completing the current loop. This forward biases the PIN diodes to provide protection. This appears schematically in Figure 2.

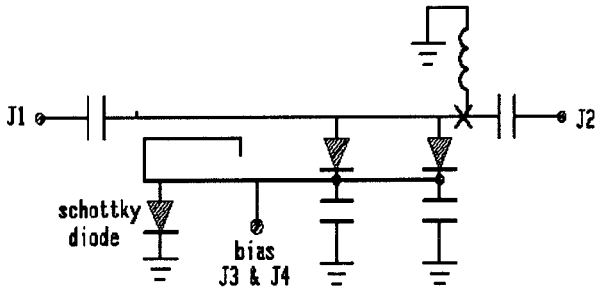

Figure 2: Receiver Protector Schematic

Glass Technology

The schematic of Figure 2 is fabricated using M/A-COM's glass technology. This process begins with a silicon wafer doped to less than 0.0035 Ω - cm. This serves as the mechanical and electrical ground plane.

The process can follow two paths. For active glass or HMIC (Heterolithic Microwave Integrated Circuit), an epitaxial layer is grown and processed to produce diodes. With no epitaxial layer, the circuit is passive glass or GMIC (Glass Microwave Integrated Circuit).

Once the glass medium is selected, the processing follows roughly the same steps. A silicon nitride layer is deposited and patterned to define the silicon via locations. The anisotropic etchant produces predictable and reproducible geometries in the single crystal silicon wafer. A feature of this process is the conical silicon vias that etch at a 54^0 angle.

The wafer is selectively etched, exposing the via sidewalls and the silicon ground plane. A silver diffusion dopes the exposed silicon to a low resistivity. This silver metallization forms the ground plane.

The next process is the application of the glass. This begins with a blanket deposition of wetting materials for glass adhesion. The glass and silicon wafers fuse under temperature and vacuum. This forms a conformal layer of glass on the wafer. This glass layer is then ground and polished to within a few μm of the silicon via top surface. The resulting planar wafer is suitable for fine line photolithography.

Metallizations are defined by a photoresist lift - off procedure. This allows difficult to etch metals such as gold and platinum to be patterned and produced with aspect ratios approaching or exceeding 1:1. The standard metallization scheme is titanium (Ti), platinum (Pt) and gold (Au), deposited by e - beam evaporation.

First, a titanium layer is deposited for adhesion. Next, platinum is incorporated as a diffusion barrier. These two processes are followed by a gold conductor layer.

A silicon nitride layer may be added at this point. This layer serves two purposes. It is the dielectric material for the fabrication of MIM capacitors on the wafer surface. It is also used as insulation over the chip surface.

The schematic of Figure 2 indicates diodes mounted on capacitors. The dielectric pattern for these capacitors is fabricated at this point. The silicon pedestal serves as the bottom plate of the capacitor. In this case, the silicon nitride layer is not etched from the silicon pedestal.

Additional layers of Ti/Pt/Au can be added at this point. They are defined using a bi - level photoresist lift - off technique. This second metal layer produces airbridge surface connections. It can also effectively double the conductor thickness, improving Q values. In this case, two additional metal layers are added, producing the top plate of the capacitor. The added metal thickness is necessary to ensure reliable solder attachment of the diodes to the capacitor.

The final frontside processing steps consist of adding layers of silicon nitride and polyimide. The silicon nitride is a passivation layer and the polyimide serves as scratch protection. These two layers can be selectively etched to expose areas where bonds or discrete elements will be attached.

Passive glass technology offers some unique advantages as a fabrication medium. The performance of the receiver protector depends largely on the PIN limiter diodes. This technology offers the flexibility to combine different discrete diodes. Diode characteristics are chosen to optimize the overall performance.

In addition, glass technology has very good power handling capabilities. The silicon vias significantly reduce the thermal path to ground. While the surrounding glass is a poor thermal conductor, silicon has a thermal conductivity that is more than 100 times better. Calculations have shown the silicon vias add only 2 - 3^0 C/W to the thermal path.

Circuit Realization

Since the chip is not monolithic and phased array radars may contain thousands of channels, high volume automated assembly and test techniques must be used. This is necessary for a cost effective solution. Automated assembly design guidelines require diode pads to be larger than the die. Bonding is with .001" diameter gold wire.

These constraints enable automatic component placement and wire bonding, but dramatically increase bond wire inductance. The diodes are represented by a series L-C-L filter structure (bond wire, junction capacitance, bond wire). Proper selection of the circuit element (blocking caps, transmission sections) values results in a bandpass filter, optimized in X - Band.

The Schottky coupled limiter needs two stages to achieve the power handling and leakage requirements. The input diode has a 10 μm I-region thickness (100 - 150V breakdown). The second stage has a 2 - 3 μm I-region (25 - 30V breakdown). The Schottky is a low barrier active glass SurMount^{TM} diode fabricated at M/A-COM's semiconductor unit.

The SurMount^{TM} Schottky diode improves reliability by eliminating bond wires. The diode has two contacts that can be soldered or epoxied to the substrate. It is fabricated with the same glass process as the substrate. This eliminates C_{te} and mechanical stress concerns when attaching the diode to the substrate.

The final layout of the receiver protector is appears in Figure 3.

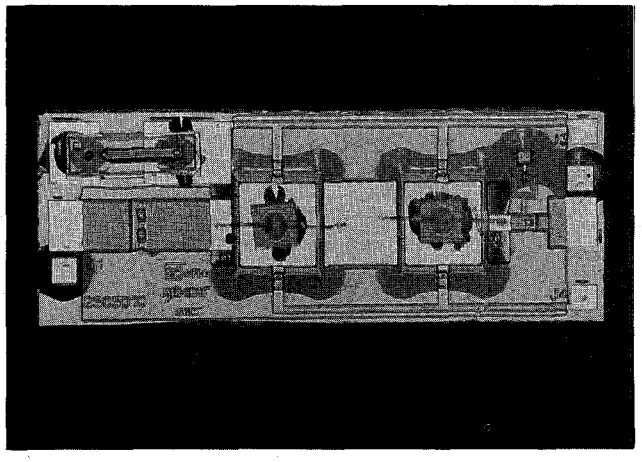

Figure 3: Layout of X-Band Receiver Protector

The chip is .010" thick. The glass portion is .008" with .002" of backside silicon. J1 and J2 are the RF ports. J3 or J4 are bias pads for active switching.

Results

Previous work [1] indicates that the active glass fabrication process results in a frequency dependent series resistance component. This phenomenon is "access resistance" and occurs because of eddy currents in the sidewall diffusion metal. The series resistance component appears in the transmission line as it approaches the silicon vias. The high conductivity silver ground plane in passive glass reduces the access resistance to 0.05 ohms/GHz.

With this assumption, the simulated insertion loss is 0.6 dB. Initial loss measurements, however, showed 1.0 dB. Analysis shows an additional component related to the proximity of the gold bond wires to the low conductivity silicon surface of the PIN diode. An updated model indicates this access resistance is as high as 0.15 ohms/GHz. This value gives good correlation to the measured data. Figures 4 & 5 show measured versus modeled results.

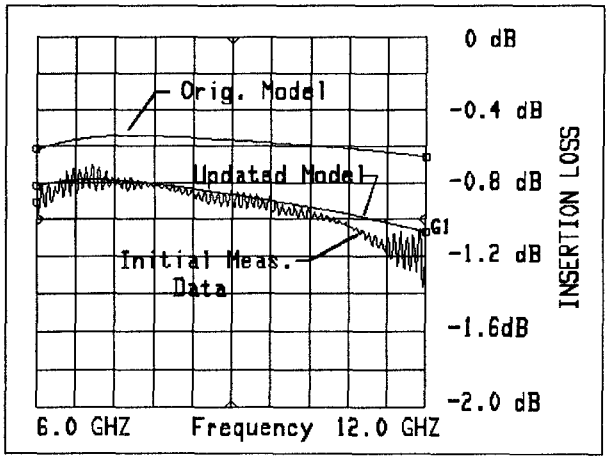

Figure 4: Measured versus Modeled Insertion Loss

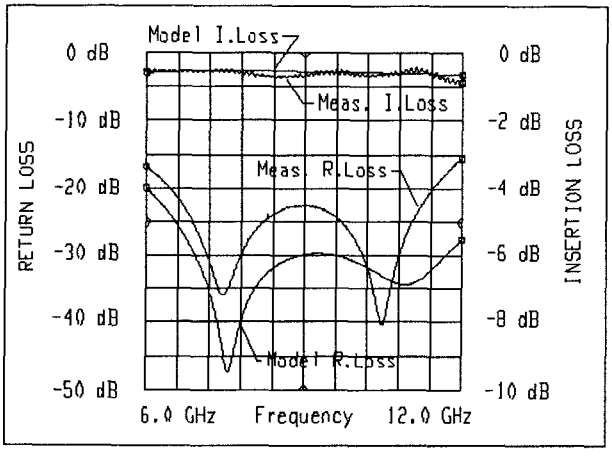

Figure 5: Measured versus Modeled Return Loss

Conclusion

M/A-COM has produced a receiver protector with high power handling capability and low insertion loss in X-Band. This device takes advantage of M/A-COM's glass technology. This technology uses batch wafer processing, automated assembly and test in high volume production. These techniques offer substantial improvement to the repeatability, reliability and manufacturability by significantly reducing the number of bonds and components.

References and Further Reading

[1] P. Onno, N. Jain, C. Souchuns, and J. Goodrich, "High Power 6-18 GHz Transfer Switch Using HMIC", M/A-COM Engineering Conference 1993.

[2] N. Jain, P. Onno, R. Keenan, "A Novel Approach for Designing High Power X-Band Matched T/R Switch-Limiter", M/A-COM Engineering Conference 1994.

[3] S. Gandhi and P. Onno, "Multithrow Switch Design Using Filter Synthesis", M/A-COM Engineering Conference 1991.

[4] C. Howell and J. Goodrich, "PIN Diode Switches on Glass Substrates ICs", **Applied Microwave**, Winter 1990.